Q.P. Code: 20EC4201 **R20**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year I Semester Regular Examinations July-2021

VLSI TECHNOLOGY

(VLSI)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Illustrate the main steps in a typical N-WELL process.	**L2**	**6M**
	b	Explain a Bi-CMOS inverter with a neat sketch.	**L2**	**6M**
		OR		
2		Derive the relation between drain to source current I_{ds}VS drain to sourcevoltage V_{ds} in non-saturated and saturated.	**L4**	**12M**

UNIT-II

3	**a**	What are the different strategies for building low powergates? Explain.	**L1**	**6M**
	b	Differentiate switch logic and gate logic.	**L4**	**6M**
		OR		
4	**a**	Explain clearly the Scalable design rules.	**L2**	**6M**
	b	Explain about static complementary gates.	**L2**	**6M**

UNIT-III

5	**a**	Draw the single row layout design.	**L2**	**6M**
	b	Briefly discuss about crosstalk minimization.	**L2**	**6M**
		OR		
6	**a**	Explain the clocking disciplines and power optimization in sequential systems.	**L2**	**6M**
	b	What are the various simulators used for combinational logic?	**L1**	**6M**

UNIT-IV

7	**a**	Briefly discuss about floor planning methods.	**L2**	**6M**
	b	Write short notes on design validation.	**L1**	**6M**
		OR		
8	**a**	Explain about placement and routing at chip level design.	**L2**	**6M**
	b	Explain about architecture testing.	**L2**	**6M**

UNIT-V

9	**a**	Explain about system on chips and embedded CPUs.	**L2**	**6M**
	b	Write notes on logic synthesis.	**L2**	**6M**
		OR		
10		With a diagram explain about detailed routing method.	**L2**	**12M**

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